Future of Power Efficient Processing

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Power Efficient Electronics are Critical to Many DoD Missions

Soldiers carry packs in 70-120 lbs range
Frequently 10-20 lbs are batteries!

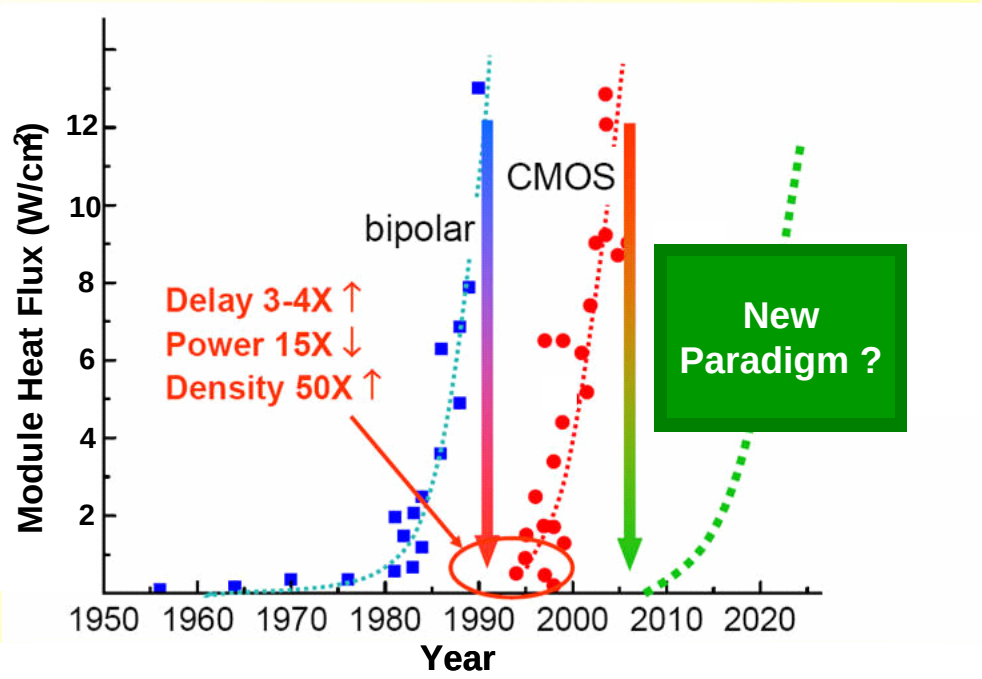
Power is frequently scarce and expensive: UAVs, remote sensor networks, space, etc.

DSRC Summer 2006
Low Power Workshop

Getting rid of dissipated heat is often a major problem by itself!

Heat pipes

Electronics History: Power Efficiency Perspective



Power = Dynamic + Static
$= 0.5CV_{dd}^2f + I_{leak}V_{dd}$

Ultimate Goals:

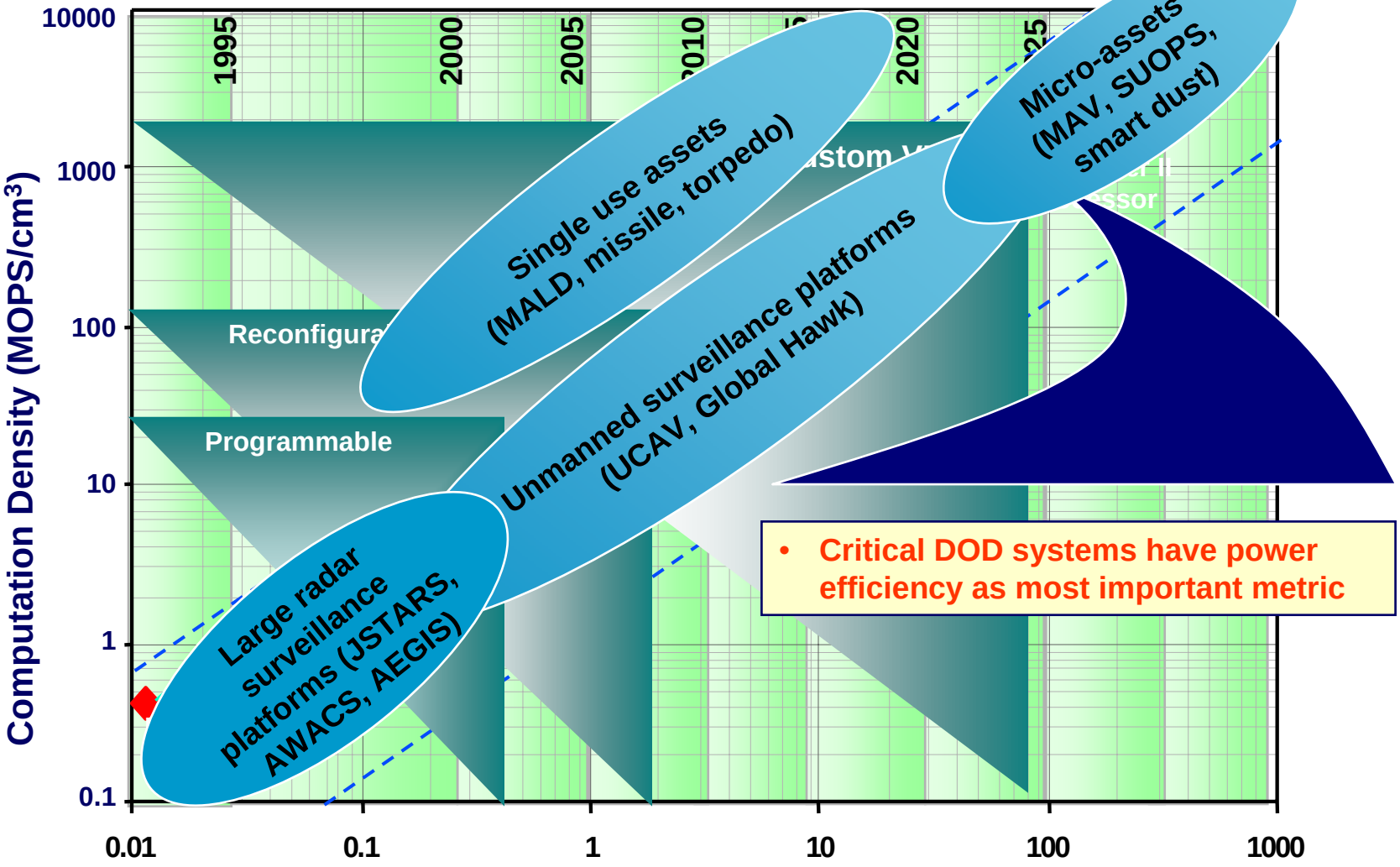
Decades power reduction
No performance penalty

- *Each technology ultimately reaches integration density limited by power dissipation*
- *Quantum jump then occurs to new technology with lower power*

Time for the next paradigm change ?

Embedded Computing for DoD

Power Efficiency (Ops/Watt) is Key

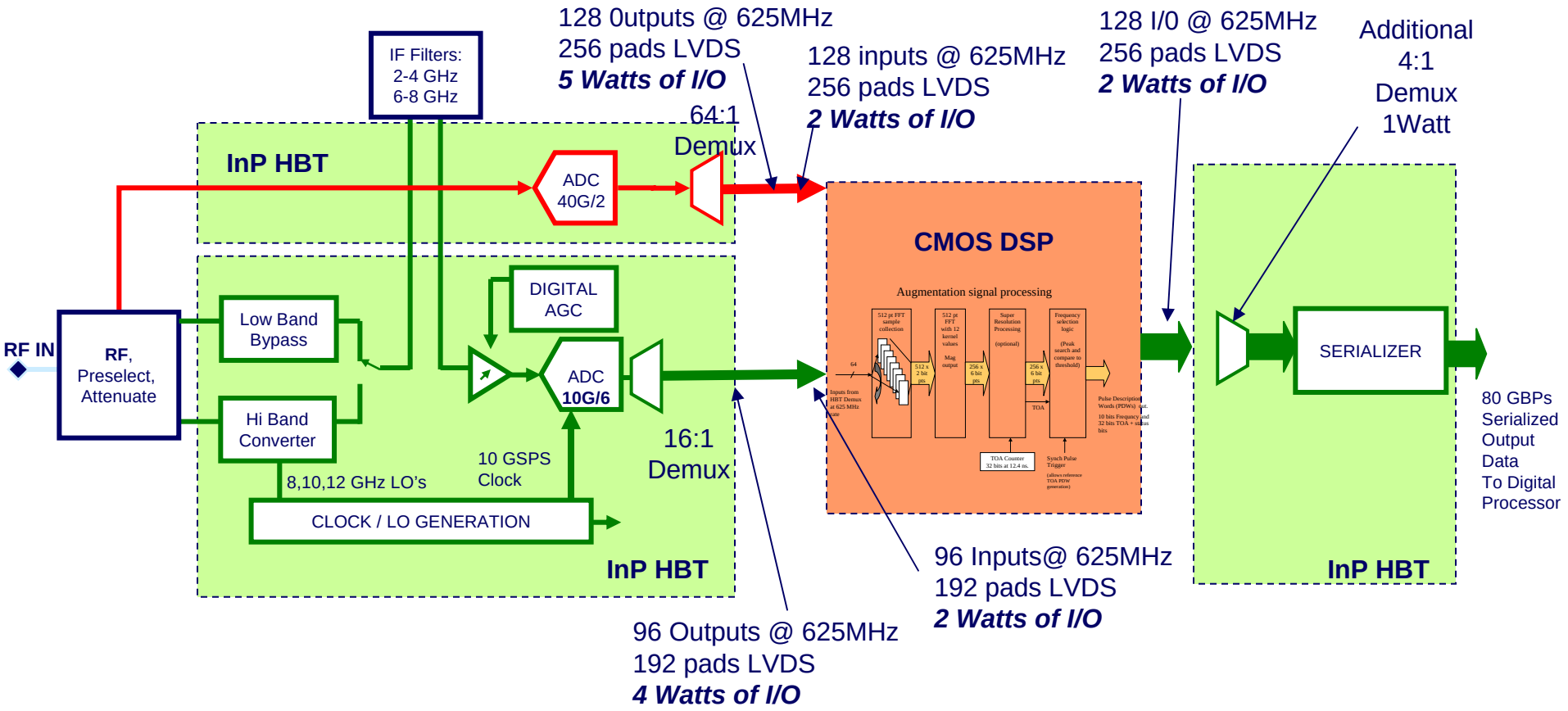


J. Anderson, MITLL Gp 102
HPEC Conference '04-'05

Some Paths Forward:
Power Efficiency

- I) Densely integrated RF technology
  - RF SOC vs MCM implementation
  - 'TEAM'
- II) Novel Architecture/Design
  - Power management
  - Sub-threshold , Parallelism, 3D
  - 'ESE', '3D-IC'
- III) Ultra-low power CMOS
  - Tunable threshold
  - Steeper sub-threshold slope (< 62 mV/dec)
  - 'STEEP' BAA coming out
- IV) Beyond Silicon
  - Carbon electronics
  - Graphene, Nanotubes
    - Workshop in early April

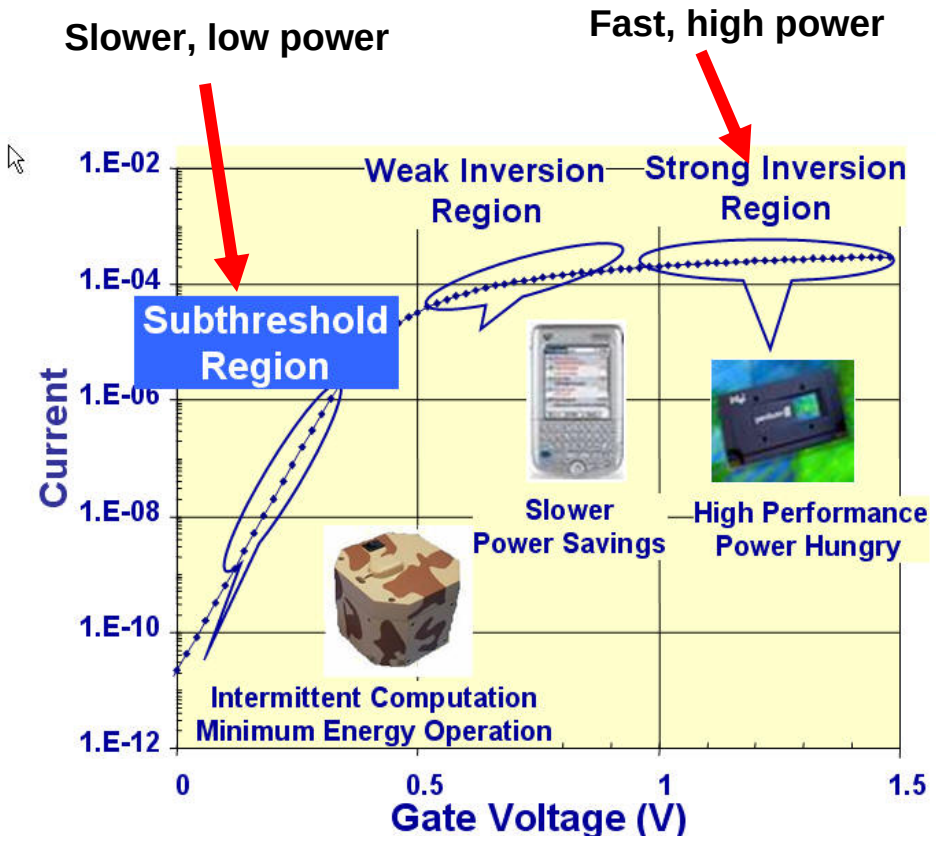
Power Benefits of Integration: RF-SOC vs. MCM



All four ICs can be implemented in a single SiGe IC

… 16 Watts of additional power due to intra-chip I/O in multi-chip approach over a monolithic implementation

Sub-threshold Digital Design:
Energy Starved Electronics (ESE) Program



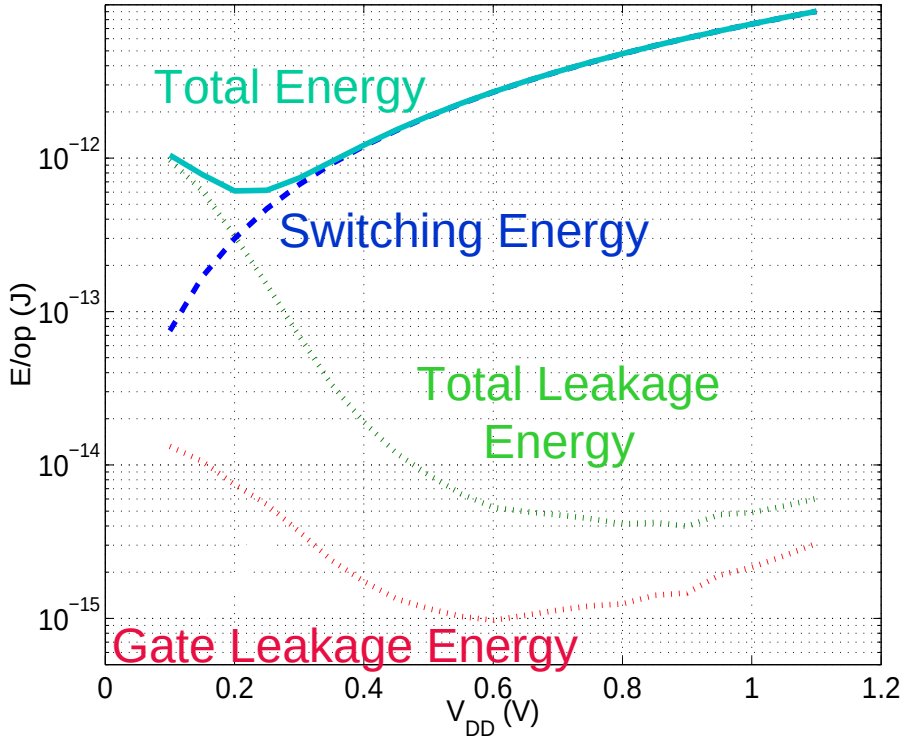
PI: Prof. Anantha Chandrakasan, MIT
Fab: TI, Dr. Dennis Buss, 65-nm CMOS

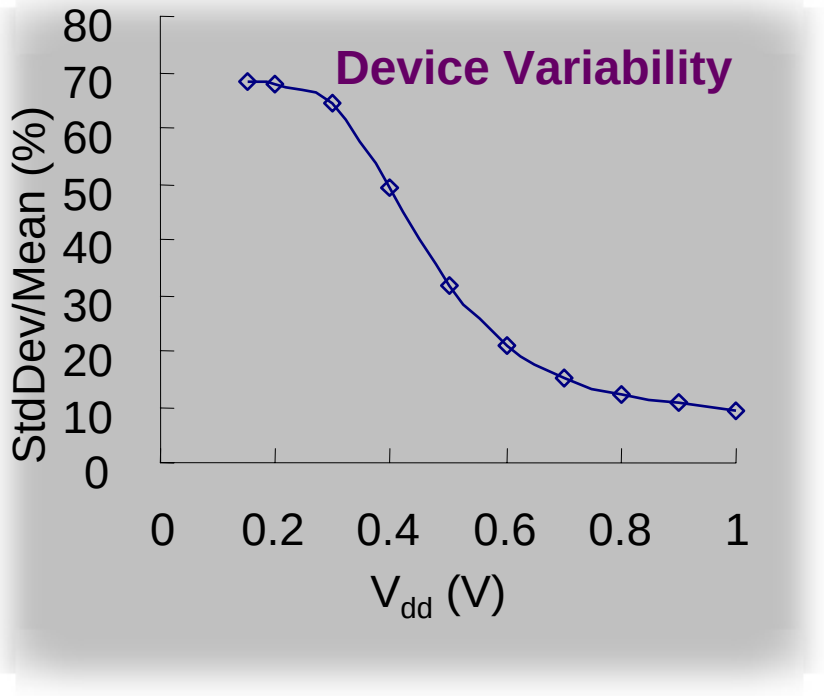
- **Goal: Enable ultra-low power digital circuits operating in the *sub-threshold regime* while maintaining adequate performance. Energy consumption savings > 10X.**

- **Technical Challenges:**
  - **Develop standard cells operating at V_{dd} < 300 mV; esp. SRAM**
  - **Achieving adequate performance (through parallelism)**
  - **Addressing high sensitivity to variations (via ECC)**

- **Design Only Approach:**
  - **No device technology changes**
  - **Exploits massive investment by industry for DoD benefit**

Minimum Energy Point:
Switching vs. Leakage





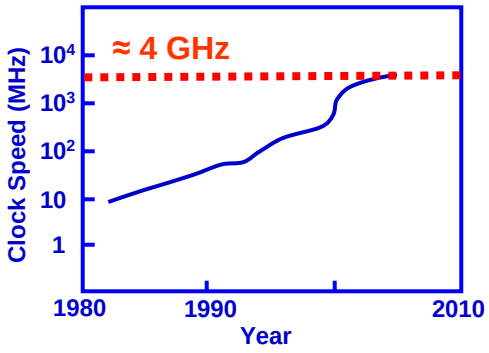
- **Minimum energy point ≈ 200 mV (sub-threshold regime)**
  - **Must be compensated for (e.g., parallelism and threshold control)**
  - **Optimum voltage V_{dd} varies with circuit activity**

- **Leakage energy increases at extremely low voltages (long delay times)**
- **Increased variability requires wider margins, reduced performance**

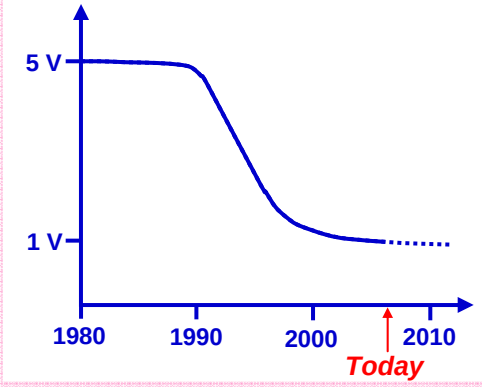
Steep-subthreshold-slope Transistors for Electronics with Extremely-low Power (STEEP)

Problem: Device Scaling alone will no longer meet DoD needs!

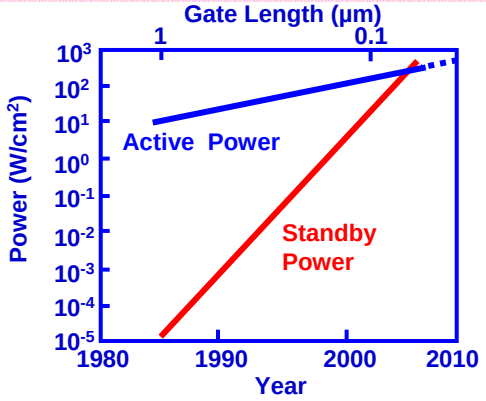
Processor speed stalled



Supply voltage stalled

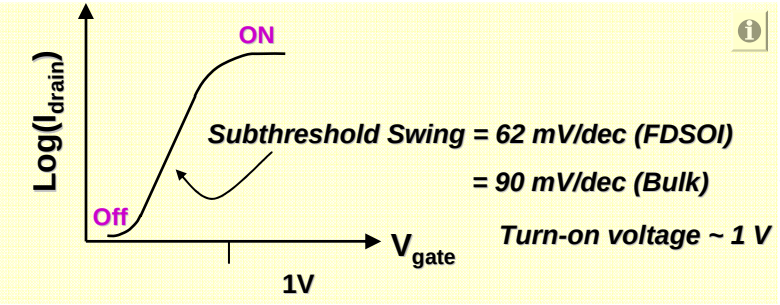


Large leakage current increase

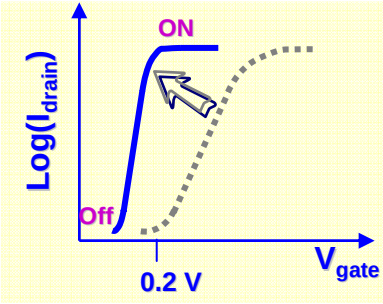


Proposed Solution: Steep-subthreshold-slope Transistors

Today



STEEP Vision



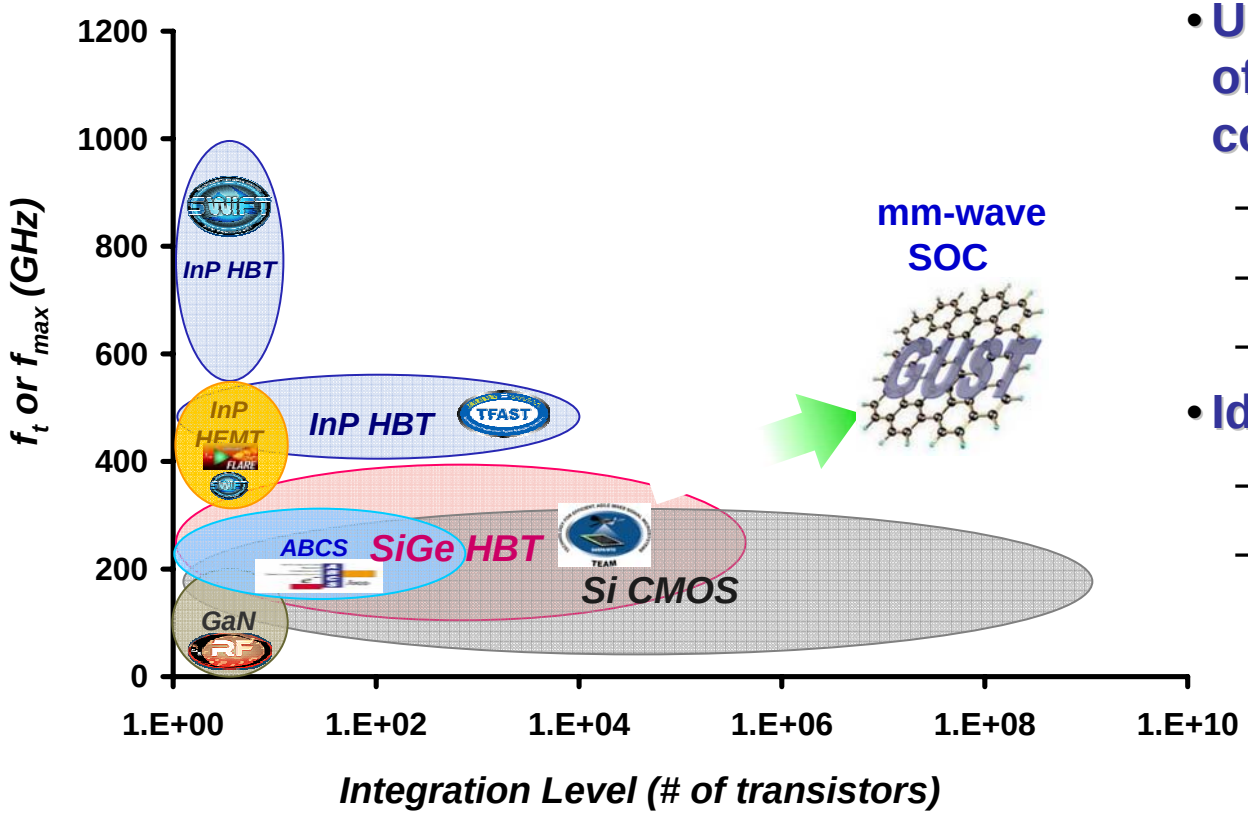
Program Goals

- Subthreshold Swing ≤ 20 mV/dec
- Turn-on voltage: ≤ 0.2 V
- 5X lower V_{DD}
- 100X lower $P_{standby}$
- 25X lower P_{active}
- **No performance penalty!**

Theoretical minimum of the subthreshold swing of MOSFET is ln10(kT/q) or 60 mV/dec

Develop ideal transistor switch for ultra-low power electronics

Carbon Electronics:
High Performance & Integration for RF-SOC's

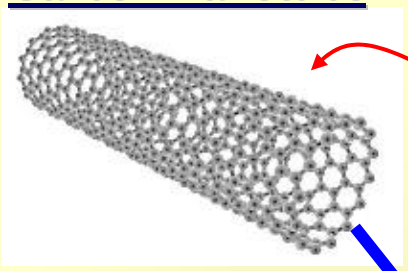


- Ultimate performance limits of mm-wave devices (radar, comms, etc):
  - *Higher speeds*
  - *Improved power efficiency*
  - *Lower "SWAP"*
- Ideal mm-wave device
  - *Key parameters*
  - *Integration path with Si*

New Opportunity: Carbon-based mm-wave SOC's

New Approach For Ideal mm-wave Material: Planar Carbon (Graphene)

Carbon Nanotube



Challenges:

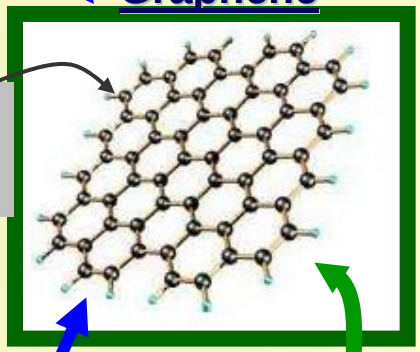
Placement & Uniformity

unroll

Graphene

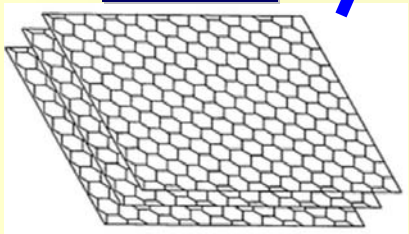
Planar system

sp^2 hexagonal
a=0.25nm, c=0.67nm
2D physics



"scrape"

Graphite



Planar form has most of the desirable properties of nanotubes

Graphene Properties:

- **High mobilities for both *electron & hole* (> 10X silicon)**
  - ***$\mu \geq 15{,}000\ cm^2/Vs$, $m^* = 0.06m_0$***
  - ***mm-wave & low power potential***
  - ***High current density***
- **Ideal electrostatics ("monolayer-on-insulator")**
  - ***Sub-nm thickness***
    - ***< Debye screening length***
  - ***Enables aggressive scaling***
- **Planar processing can be used**
  - ***Standard paradigm***
  - ***Straightforward integration with CMOS***

Semimetal band structure

- ***I_{on}/I_{off} ~ 30, useful for RF devices***

Graphene is very promising material for mm-wave RF-SOC technology

A Possible Path Forward